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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/626,767

07/25/2003

Woon-Yong Park

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1856

7590

06/16/2004

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EXAMINER

CHUNG, DAVID Y

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/626,767	<b>Applicant(s)</b> PARK ET AL.	
	<b>Examiner</b> David Y. Chung	<b>Art Unit</b> 2871	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 24-36 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 24 and 25 is/are rejected.
- 7) ☒ Claim(s) 26-36 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/779,705.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claim 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. (U.S. 5,929,958) in further view of Tanaka et al. (U.S. 4,960,719).**

Ohta et al. discloses a parallel field liquid crystal display device having wide viewing angle characteristics. Note in figure 2, the gate lines GL, data lines DL, counter voltage signal lines CL, common electrodes CT, and pixel electrodes PX. See column 12, line 25 – column 13, line 65. Note in figure 8, the TFT structure comprising gate electrode GT, gate insulating film GI, semiconductor layer AS, source electrode SD1, and drain electrode SD2. See column 16, lines 28-53. In figure 8, layer d0 is doped with phosphorous for ohmic contact. See column 17, lines 50-56. Note in figures 12A and 12B, the structure of the gate insulating film GI near the external gate connection terminals GTM. The gate insulating film is formed on the right side of the boundary line shown in figure 12A in order to expose the gate terminals. See column 22, line 53 – column 23, line 47.

Ohta et al. does not disclose using a mask to prevent deposition of the gate insulating film onto the gate terminals. Tanaka et al. (U.S. 4,960,719) discloses that it was conventional for the sake of simplicity to expose the gate terminal by using the metal mask 32 shown in figure 9 during the formation of the gate insulating film and other layers. The metal mask shown in figure 9 prevents the gate insulating film and other layers from being deposited on the gate terminals. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a mask to prevent deposition of the gate insulating film onto the gate terminals for the sake of simplicity as taught by Tanaka et al. (U.S. 4,960,719).

**Claims 25 and 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. (U.S. 5,929,958) in further view of Tanaka et al. (U.S. 4,960,719) and Tanaka et al. (U.S. 5,065,202).**

As to claim 25, Ohta et al. discloses the structure of the device around the data terminals DTM in figure 13A and 13B. See column 23, line 49 – column 24, line 60. Note that the gate insulating film GI is formed to the right of the boundary line shown in figure 13A.

Ohta et al. does not disclose exposing the data terminals by using a mask to prevent deposition of the gate insulating film or other layers. Tanaka et al. (U.S. 5,065,202) discloses that when the conventional mask discussed above (shown here in figure 10) is used to form the gate insulating film, the gate insulating film is also not

formed on the data terminals, as shown in figure 11. See column 2, lines 9-32. It would have been obvious to one of ordinary skill in the art at the time of invention to expose the data terminals using a mask to prevent deposition of the gate insulating film and other layers for the sake of simplicity as discussed regarding claim 24.

As to claim 36, Ohta et al. discloses the structure of the passivation layer in the areas of the gate terminals and data terminals in figures 12A, 12B, 13A and 13B. The passivation layer is formed to the right of the boundary lines shown in figures 12A and 13A.

Ohta et al. does not disclose forming the passivation layer PSV using the mask disclosed in either of the Tanaka et al. references. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use the mask disclosed by the Tanaka et al. references to prevent deposition of the passivation layer on the gate and data terminals for the sake of simplicity. This would reduce the complexity of the manufacturing process by allowing the passivation layer to be formed using a single manufacturing step, instead of requiring a separate photolithography and etching step to remove the layer from the terminal areas.

#### ***Allowable Subject Matter***

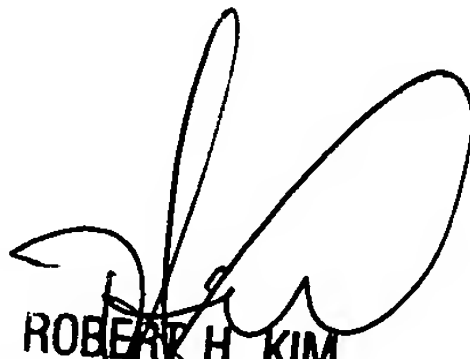
Claims 26-35 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2871

The following is a statement of reasons for the indication of allowable subject matter: the prior art did not teach or suggest forming the various elements recited in claim 24 using a photolithography process which uses one photoresist pattern having portions with different thickness.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Chung whose telephone number is (571) 272-2288. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

  
ROBERT H. KIM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800